REMARKS

Reconsideration of the application, as amended, is respectfully requested.

I. STATUS OF THE CLAIMS

Claims 1-33 are currently pending. Claims 1-3, 13-14, 21, 23 and 28-29 have been amended herewith to provide even more specific language than the expression "in a direction of" in these claims in order to expedite the prosecution of the present application. Moreover, claims 1 and 21 have been amended to further clarify that the storage electrodes formed on the storage electrode contact bodies are arranged in a zigzag pattern along at least one of the bit lines or the gate lines.

Support for the above amendments may be found throughout the specification as originally filed. No new matter has been added by virtue of this amendment.

II. 35 U.S.C. 112, SECOND PARAGRAPH REJECTIONS

Claims 1-3, 13-14, 21, 23 and 28-29 have been rejected under 35 U.S.C. 112, second paragraph on the grounds that the expression " in a direction of" recited in these claims renders these claims indefinite.

As stated in the previous response, Applicants respectfully disagree with the Examiner that the expression "in a direction of" as recited in the above claims is indefinite. However, in order to expedite the prosecution of the present application, claims 1-3, 13-14, 21, 23 and 28-29 have been amended herewith to provide even more specific language than the expression "in a direction of" in these claims.

In view of the above action taken, it is believed that the above rejections have been obviated. Therefore, withdrawal of the above rejection to claims 1-3, 13-14, 21, 23 and 28-29 is requested.

III. 35 U.S.C. 102(e) and 35 U.S.C. 103(a) REJECTIONS

(i) Claims 1-4, 6-12, 15-18, 21-27, 30 and 31 have been rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,403,413 to Hayano et al. ("the Hayano patent").

(ii) Claims 5, 13, 14, 28 and 29 have been rejected under 35 U.S.C. 103(a) as being obvious over Hayano (as discussed above) in view of U.S. Patent Application Publication No. 2001/0045589 to Takeda et al.

(iii) Claims 19, 20, 32 and 33 have been rejected under 35 U.S.C. 103(a) as being obvious over Hayano (as discussed above) in view of U.S. Patent Application Publication No. 2001/0041406 to Goebel et al. ("the Goebel publication").

In order for a claim to be rendered unpatentable by the cited art, the cited art must either (i) anticipate the claim or otherwise (ii) render the claim obvious. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. **(See MPEP 2133, Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).** Alternatively, to establish prima facie obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the cited reference or references. **(See MPEP 2143.03; In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)).**

However, Hayano, Takeda and/or Goebel alone or in combination each fail to teach or suggest all of the features recited in independent claims 1 and 21.

As mentioned above, method claims 1 and 21 have been amended to further clarify that the storage electrodes formed on the storage electrode contact bodies are arranged in a zigzag pattern along at least one of the bit lines or the gate lines.

In particular, Hayano, Takeda and/or Goebel each at the very least fail to teach or suggest a method for manufacturing a semiconductor device, which includes forming a storage

electrode on each of the storage electrode contact bodies, wherein the storage electrodes formed on the storage electrode contact bodies are arranged in a zigzag pattern along at least one of the bit lines or the gate lines, as essentially recited in claims 1 and 21. For example, exemplary embodiments of the present invention which are within the scope of claims 1 and 21 describe and illustrate storage electrodes 900 arranged in a zigzag pattern along at least one of the bit lines 600 or the gate lines 200 . **(See pages 17-20 and Figs. 10A-10C of the present specification).** In contrast, Hayano, Takeda and/or Goebel are each completely silent regarding forming a storage electrode on each of the storage electrode contact bodies, wherein the storage electrodes formed on the storage electrode contact bodies are arranged in a zigzag pattern along at least one of the bit lines or the gate lines , as essentially recited in claims 1 and 21. Thus, Hayano, Takeda and/or Goebel each fail to teach or suggest all of the features recited in claims 1 and 21.

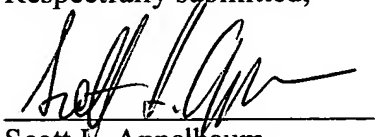
Moreover, it would not have been obvious to one skilled in the art to form storage electrodes on storage electrode contact bodies, wherein the storage contact electrodes are arranged in a zigzag pattern along at least one of the bit lines or the gate lines, as essentially recited in claims 1 and 21. It is well known that pursuant to the U.S. patent laws, a showing of a long felt-need or the failure of others in an industry to solve a particular difficulty may be used for rebutting obviousness. **(See MPEP 2144.05)** For example, as discussed in the present specification, despite numerous attempts, the conventional art has failed to provide a particular arrangement for the storage electrodes of a semiconductor device which prevents twin bit failure between the storage electrodes. **(See pages 3 and 4 of the present specification).** In contrast, the forming of a storage electrode on each of the storage electrode contact bodies, wherein the storage electrodes formed on the storage electrode contact bodies are arranged in a zigzag pattern along at least one of the bit lines or the gate lines , as essentially recited in claims 1 and 21 does prevent the collapsing of storage electrodes, thereby also preventing twin bit failure. **(See page 17, lines 24-26 of the present specification).** Accordingly, it is clear that the methods recited in claims 1 and 21 achieve what the conventional art has failed to by providing an arrangement for the storage electrodes (a zigzag pattern arrangement) along at least one of the bit lines or the gate lines which prevents twin bit failure. Thus, it would not have been obvious to one skilled in the art to utilize a method which provides the above zigzag pattern arrangement for storage electrodes of a semiconductor device as essentially recited in claims 1 and 21.

Therefore, for at least the reasons set forth above, claims 1 and 21 are patentable over each of the above cited references of Hayano, Takeda and/or Goebel. Moreover, as claims 2-20 depend from and incorporate all of the limitations of claim 1 and claims 22-33 depend from and incorporate all of the limitations of claim 21, these dependent claims are likewise patentable over all of the above cited references.

IV. CONCLUSION:

For the foregoing reasons, the present application, including claims 1-33, is believed to be in condition for allowance. The Examiner's early and favorable action is respectfully requested. The Examiner is invited to contact the undersigned if he has any questions or comments in this matter.

Respectfully submitted,



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